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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission: 34

Application Number	09/829,587
Filing Date	04/09/2001
First Named Inventor	Pavel N. Laptev
Art Unit	1763
Examiner Name	Zervigon, Rudy
Attorney Docket Number	TEGL-01212US0

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
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- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
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- [ ] Terminal Disclaimer
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- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
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- [ ] Status Letter
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Fliesler Meyer, LLP Customer No.: 23910		
Signature			
Printed name	Michael L. Robbins		
Date	9/13/06	Reg. No.	54,774

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Typed or printed name	Michael L. Robbins	Date	9/13/06

Attorney Docket No.: TEGL-1212US0
MRobbins/TEGL/1212US0/1212US0.Trans.Resp.Appeal

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FEE TRANSMITTAL For FY 2006

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) -0-

Complete if Known	
Application Number	09/829,587
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First Named Inventor	Pavel N. Laptev
Examiner Name	Zervigon, Rudy
Art Unit	1763
Attorney Docket No.	TEGL-01212US0

METHOD OF PAYMENT (check all that apply)

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☑ Deposit Account Deposit Account Number: 06-1325 Deposit Account Name: Fliesler Meyer LLP

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1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): _____	

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 54,774	Telephone 415-362-3800
Name (Print/Type)	Michael L. Robbins		Date 09/13/06

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application Inventor(s): Laptev, P. Appln. No.: 09/829,587 Confirm. No.: 7932 Filed: April 9, 2001 Title: System for, and Method of, Etching a Surface on a Wafer	PATENT APPLICATION Art Unit: 1763 Examiner: Rudy Zervigon **Customer No. 23910**

CERTIFICATE OF FACSIMILE TRANSMISSION UNDER 37 C.F.R. § 1.8

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(Attorney Signature)
Michael L. Robbins, Reg. No. 54,774
Signature Date: 9/6/06

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REPLY BRIEF IN RESPONSE TO EXAMINER'S ANSWER

Sir:

Appellant submits this Brief for consideration by the Board of Patent Appeals and Interferences following the EXAMINER'S ANSWER mailed on July 13, 2006. Appellant submitted a Notice of Appeal along with the appropriate fee on October 9, 2003.

I. REAL PARTY IN INTEREST

Sputtered Films, Inc., the assignee of record of the application.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1-21 and 43-51 have been rejected by the Examiner on the basis of prior art cited by the Examiner. Claims 22-42 have been withdrawn from prosecution in the application. Claims 1-51 have been, and are, the only claims in the application. The rejection of claims 1-21 and 43-51 is being appealed.

IV. STATUS OF AMENDMENTS

Applicant filed a proposed amendment under Rule 116 on October 30, 2003 to amend one (1) word in each of claims 1, 3, 8, 48 and 49, so as to make the claims consistent with the disclosure in the specification and the drawings. In an Office Action dated 11/07/2003, the Examiner refused to enter the proposed amendment on the ground that applicant's amendment to claim 3 changing "less" to -- greater -- "requires additional consideration of the cited prior art." Applicant has accordingly written claims 1, 3, 8, 48 and 49 in this Supplemental Appeal Brief without including applicant's proposed changes in the claims.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Specification from page 7, line 3 through page 15, line 17

Figures 1-4 show a preferred embodiment, generally indicated at 10, of apparatus for etching a surface 12 of an insulating layer 14 in a wafer generally indicated at 16. As will be appreciated, the wafer may be formed from a plurality of stacked layers, some of them electrically conductive and others electrically insulating. In addition to the insulating layer 14, an electrically conductive layer 15 and an electrically insulating base layer 17 are schematically shown to represent the different layers in the integrated circuit chip. The insulating layer 14 may have a plurality of grooves or sockets 18. The

insulating layer 14 may illustratively be made from a suitable material such as a polyamide.

The insulating layer 14 may illustratively have a thickness of approximately three (3) microns. The sockets 18 may be completely, or partially, formed through the thickness of approximately three (3) microns in the insulating layer 14. Figure 2 illustratively shows the sockets 18 as extending completely through the thickness of the insulating layer 14. The preferred apparatus 10 of this invention illustratively may etch approximately one hundred angstroms (100 Å) from the surface 12 of the insulating layers 14 in a smooth and even layer and without any pits in the layer.

The apparatus 10 includes an enclosure 20 which may be formed in part by an electrode 22, and electrode 24 displaced from, but preferably substantially parallel to, the electrode 22 and magnets 26 and 28 disposed in a transverse (preferably substantially perpendicular) relationship to the electrodes 22 and 24. The electrode 22 is disposed in a contiguous but spaced and substantially parallel relationship to the wafer 16 and is movable in position toward or away from the wafer, as indicated by a double-headed arrow 25. The spacing between the wafer 16 and the electrode 22 may illustratively be in the order of 0.1 - 2mm. A plate 30 extending from the magnet 28 in a substantially parallel and adjacent, but spaced, relationship to the electrode 22 also defines the enclosure 20. A ring 32 extending from the magnet 26 to a position spaced from, but adjacent to, the electrode 24 also defines in part the enclosure 20. The plate 30 and the ring 32 may be considered as electrical conductors.

The magnets 26 and 28 preferably constitute permanent magnets but they may also constitute magnetizable members on which windings are disposed to produce a saturable magnetic flux when a current flows through the windings. The magnets 26 and 28 may have a north polarization (indicated by the letter "N" in Figure 1) at their positions of contiguity and may have a south polarization (indicated by the letter "S" in Figure 1) at their opposite ends. The magnets 26 and 28, the plate 30 and the ring 32 are provided with a reference potential such as a ground 34. The wafer 16 is disposed in close proximity to the electrode 22 within the enclosure 20 and in substantially parallel relationship to the electrode. The wafer 16 is at a floating potential.

The electrode 22 receives a relatively low AC voltage from a power supply 36 at a suitable frequency such as approximately 13.56 MHz. As will be explained in detail subsequently, this causes the electrode 22 to receive a relatively low negative DC bias such as a negative bias in the order of -100 volts to -500 volts. A matching network 38 is preferably disposed electrically between the power supply 36 and the electrode 22 to match the impedance of the power supply to the impedance of the electrode.

The electrode 24 receives a relatively high AC voltage from a power supply 40 at a suitable frequency such as approximately 13.56 MHz. As will be explained in detail subsequently, this causes the electrode 24 to have a relatively high negative DC bias such as a negative bias in the order of -1000 volts to -3000 volts. A matching network and zero bias circuit 42 are preferably disposed electrically between the power supply 40 and the electrode 24 to match the impedance of the power supply to the impedance of the electrode and to provide substantially a ground potential on the electrode. The zero bias circuit may constitute an inductance between the electrode 24 and ground to provide a high impedance for alternating voltages and to provide a low impedance for a DC voltage. The power supplies 36 and 40 may constitute a single power supply.

A conduit 44 is provided for introducing molecules of an inert gas such as argon into the enclosure 20 from a source 45. The argon molecules pass into the enclosure 30 through the space between the electrode 24 and the ring 32. The argon molecules pass out of the enclosure 20 through the space between the plate 30 and the wafer 16. The argon gas flow through the enclosure 30 may illustratively be at a flow rate of 0.1-50 SCCM at a working pressure of 0.5-5mTorr. The movement of the argon molecules through the enclosure 20 is facilitated by a vacuum pump 47.

A negative bias is produced on the electrode 22 because of the alternating voltage applied to the electrode. In the positive half cycles of the alternating voltage, the electrode 22 attracts electrons because of the electrical field between the electrode and the ground potential 34 on the plate 30. In the negative half cycles of the alternating voltage, positive ions are attracted to the electrode because of the electrical field between the electrode and the ground potential 34 on the plate 30. Since the electrons are considerably lighter in weight than the positive ions, they move faster toward the

electrode 22 than the positive ions. This causes the electrons to accumulate in the space adjacent the electrode 22, thereby producing the negative DC bias on the electrode. The electrode 24 receives a negative bias because of the same physical phenomenon. However, the negative bias on the electrode 22 is considerably less than the negative DC bias on the electrode 24 because of the differences in the voltages applied to the electrodes.

As previously indicated, the magnetic field produced by the magnets 26 and 28 is substantially perpendicular to the electrical fields produced by the electrodes 22 and 24. This causes electrons in the enclosure 20 to move in a spiral or helical path between the electrode 22 and the plate 30, and between the electrode 24 and the ring 32, because of the ground potentials on the plate and the ring. The electrons strike molecules of argon gas and ionize these molecules. Since the electrical field between the electrode 24 and the ring 32 is considerably stronger than the electrical field between the electrode 22 and the plate 30, most of the ionization of argon molecules occurs in the region of the electrode 24. Some of these argon ions then move into the region of the electrode 22.

Figure 3 illustrates at 46 lines of force produced by the electrical field between the electrode 22 and the plate 30. Arrows indicate the direction of the lines 46 of force. The electrons in the enclosure 20 travel in a spiral or helical path along the force lines 46, the spiral or helical path resulting from the force of the magnetic field as the electrons move along the force lines 46. In like manner, Figure 3 illustrates at 48 lines of force produced by the electrical field between the electrode 24 and the ring 32 and between the electrode and the grounded magnets 26 and 28. The electrons in the enclosure 20 travel in a spiral or helical path along the force lines 48 because of the force on the electrons by the magnets 26 and 28.

Applicant's assignee of record in this application has previously sold one (1) unit of apparatus with features similar to the apparatus shown in Figure 1. This unit may have been sold more than one (1) year prior to the date of this application. However, there is one significant difference between the apparatus 10 constituting the preferred embodiment of the invention and the unit previously sold by applicant's assignee. The significant difference is that the wafer 16 engaged the electrode 22 in the one (1) unit sold

prior to the date of this application. The circuit equivalent of this arrangement is shown in Figure 5b and is indicated as prior art in that Figure. As previously indicated, the wafer 16 is separated from the electrode 22 in the preferred embodiment 10 of this invention.

As will be seen, the combination of the electrode 22 and the wafer 16 in Figure 5a is seen as a single electrode or plate in a capacitor 50 in Figure 5b. The other electrode or plate in the capacitor 50 is defined by the positive ions in the enclosure 20 at positions adjacent the electrode 24. These positive ions are schematically illustrated by dots (.) at 51 in Figure 3. The dielectric between the plates of the capacitor 50 may be considered to be the insulating layer 14. The impedance of the capacitor 50 is accordingly relatively low because the insulting layer 14 is relatively thin and because the dielectric constant of the insulating layer is lower than the dielectric constant of air or the dielectric constant of a vacuum.

Since the impedance of the capacitor 50 is relatively low, a relatively large current flows through the capacitor. This current results from the attraction of the argon ions to the insulating layer 14 because of the negative DC voltage on the electrode 22. The relatively large current produces an etching of molecules and ions from the surface 12 of the insulating layer 14. This etching is of such a force that the etching is not smooth, even or uniform. Pitting of the surface of the insulating layer 14 accordingly occurs. The problem is particularly aggravated in considering the etching of the walls of the sockets 18 in the insulating layer 14.

Since the etching does not result in a smooth, even and uniform surface 12 of the insulating layer 14, any subsequent deposition of an electrically conductive layer on the surface 12 has significant differences in thickness of the electrically conductive material at different positions on the surface 12. This significantly affects the electrical characteristics of the electrical deposition on the insulating layer 14 and produces significant deterioration in the performance characteristics of the integrated circuit chips formed from the wafer.

As previously indicated, the wafer 16 is separated from the electrode 22 in the preferred embodiment 10 of this invention. The separation may be in the order of 0.1 to 2.0 millimeters. This causes two (2) capacitors 52 and 54 in Figure 4b to be defined by

the electrode 22, the wafer 16 and the charge produced by the argon ions 5 1 in the enclosure 20 in the vicinity of the electrode 22. The plates of the capacitor 52 in Figure 4b may be respectively considered to be defined by the electrode 22 and by the electrically conductive deposition layers in the wafer 16. Although there may be argon ions in this gap, the argon ions are relatively small in number. Furthermore, the gap is so small that the argon ions cannot be accelerated to any significant degree. Because of these factors, the dielectric in the capacitor 52 in Figure 4b may be considered to be the gap between the electrode 22 and the wafer 16. This gap causes the impedance of the capacitor 52 to be relatively high. This impedance can be adjusted to any desired value by adjusting the position of the electrode 22 in the opposite directions 25 to vary the distance between the electrode and the wafer 16.

The capacitors 52 and 54 may be considered to be in series as shown in Figure 4b. The capacitor 54 may be considered to have plates defined by the electrically conductive layers in the wafer 16 and by the charge provided by the argon ions 5 1 in the enclosure 20 in the vicinity of the electrode 22. The dielectric for the capacitor 54 may be considered to be the insulating layer 14. The impedance of the capacitor 54 is relatively low, particularly in relation to the impedance of the capacitor 52, because of the thin dimension of the insulating layer 14 and the dielectric constant of the insulating layer.

The current through the series circuit including the capacitors 52 and 54 in Figure 4b is limited and controlled by the capacitor 52 because of the high impedance of the capacitor. This limited and controlled current provides a gentle etching of the surface 12 of the insulating layer 14 and of the walls of the sockets 18. As a result, any specified amount of material may be etched from the surface 12 of the insulating layer 14 and from the walls of the sockets 18. For example, an etching of the material of the insulating layers 14 and the walls of the sockets 18 may be provided in a thickness of approximately one hundred Angstroms (100 Å).

The etching produces smooth, even and uniform surfaces of the insulating layer 14 by the apparatus 10 as a result of the etching. This provides for a deposition of a smooth, uniform and even thickness of an electrically conductive material on the etched surface of the insulating layer 14. The etching of the walls in the sockets 18 is also even, uniform

and smooth. This constitutes a distinct advance over the prior art, even the prior art as represented by the single unit of the apparatus sold by applicant's assignee prior to the filing date of this application, this prior unit being shown in Figure 5a and being represented by the electrical circuitry shown in Figure 5b.

As shown schematically in Figure 4a, the balls 60 made from a suitable material such as copper may be provided on the electrically conductive surface of the wafer 160. The balls 60 operate as electrical leads. The balls 60 are known in wafers of the prior art. The balls 60 are not affected by the actions of the capacitances 52 and 54 in Figure 4b.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Examiner has provided the grounds of rejection as follows:

A. Rejection of claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 50 under 35 U.S.C. 102(b) as being anticipated by Koshimizu (U.S. Patent 5,980,687) and demonstrated by Mountsier (U.S. Patent 5,810,933).

B. Rejection of claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49, and 51 under 35 U.S.C 103(a) as being unpatentable over Koshimizu (U.S. Patent 5,980,687) in view of Mountsier (U.S. Patent 5,810,933).

C. Rejection of claims 1-21, and 43-51 under 35 U.S.C 103(a) as being unpatentable over Applicant's own admitted prior art in view of Mountsier (U.S. Patent 5,810,933).

VII. ARGUMENT IN RESPONSE TO EXAMINER'S ANSWER.

A. Rejection of claims 1-4, 7-9, 11, 14-16, 19-21, 43-47, and 50 under 35 U.S.C. 102(b) as being anticipated by Koshimizu (5,980,687) and demonstrated by Mountsier et al. (5,810,933).

Applicant clarify in this Reply that the invention disclosed in the present application is the spaced relationship of the wafer from the electrodes, which provides a smoother surface on the wafer after etching.

Applicant submits that Koshimizu does not provide a spaced relationship between the electrodes and the wafer. As argued in the **FIFTH SUPPLEMENTAL APPEAL**

BRIEF, Figs. 1 and 3 of Koshimizu clearly show that the wafer W is either attached to the electrode 116 or attached to the electrode 110. Further, Koshimizu also discloses that the wafer W is fixed on the surface of either electrode 110 or 11.

In the **EXAMINER'S ANSWER**, the Examiner writes that "[i]n response, the Examiner emphasizes that the claimed invention does not specify the word 'separation' in any of the finally rejected claims. Applicant does claim a 'spaced' relationship between the wafer and an electrode surface. As a result, Applicant's above-quoted arguments do not address the Examiner's rejections of the claimed invention...although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. (See MPEP § 2145, § 2111 - § 2116.01; In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993); Constant v. Advanced Micro-Devices, Inc., 848 F2d 1560, 1571-72, 7 USPQ2d 1057, 1064-1065 (Fed. Cir.), cert. denied, 488 U.S. 892 (1988); Ex parte McCullough, 7 USPQ2d 1889, 1891 (Bd. Pat. App. & Inter. 1987)."

The Applicant concedes that, as recited in MPEP § 2111.01, "[w]hile the meaning of claims of issued patents are interpreted in light of the specification...this is not the mode of claim interpretation to be applied during examination." However, MPEP § 2111.01 further states that "[t]his means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification."

The Applicant interprets the **EXAMINER'S ANSWER** as asserting that the specification ***does not*** provide a clear definition of the term "spaced"; and that therefore the term "spaced" should be interpreted to include the relationship illustrated in Figure 5 and 6 of *Mountsier* '933. The Applicant acquiesces to an interpretation by the Examiner of the rule recited in MPEP § 2111.01 that would assign the plain meaning to the word "spaced," where the specification does not provide a clear definition. However, the Applicant asserts that the plain meaning of the word "spaced" is equivalent to the word "separated," and that as such, the Applicant's arguments in the **FIFTH SUPPLEMENTAL APPEAL BRIEF** address the Examiner's rejections of the claimed invention.

According to *The American Heritage Dictionary of the English Language* 1725 (3d ed. 1992), the definition of "spaced", as recited for the transitive verb form of "space" is

1. To organize or arrange with spaces between.
2. To separate or keep apart.

Applicant submits that the wafer and electrode of Figures 5 and 6 of *Mountsier* '933, and the accompanying description, do not teach or disclose a wafer and electrode organized or arranged with spaces between (them), or a wafer and electrode separated or kept apart. The wafer and electrode are shown in contact. The occasional gaps between the wafer and portions of the electrode pointed out by the Examiner do not satisfy the recitation that the wafer be separated or kept apart from the electrode. The Examiner's analysis would seem to read claim 1 as if claim 1 were amended to recite "a second electrode biased to a second voltage lower than the first voltage and spaced from the first electrode and a portion of the second electrode spaced from the wafer and further spaced from the wafer than the first electrode." Interpreting claim 1 in this fashion would seem to be no less an unreasonably semantic argument than an argument asserting that the bottom surface of the electrode is spaced from a top surface of the wafer, which is no doubt true.

Thus Applicant reasserts that for the above reasons and those reasons presented in the **FIFTH SUPPLEMENTAL APPEAL BRIEF**, independent claims 1, 7, and 21, are not anticipated by *Koshimizu '687* and demonstrated by *Mountsier* '933. Dependent claims 2-4, 8, 9, 11, 43-47, and 50 ultimately depend from one of claim 1, 7, and 21, and therefore include all of the limitations of the base claim. As such, *Koshimizu '687* as demonstrated by *Mountsier* '933 fails to anticipate claims 2-4, 8, 9, 11, 43-47 and 50.

The Examiner writes that "with respect to Applicant's claim 14 argument...the Mountsier et al (USPat. 5,810,933) patent demonstrates the established knowledge in the art of gap(s) and spacing(s) between the wafer and its support surface, claimed features of the claimed apparatus are presumed to prove inherency. When the structure recited in the references is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Where the claimed and prior art products are identical or

substantially identical in structure or composition, or are produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA1977)." For the reasons given above and in the **FIFTH SUPPLEMENTAL APPEAL BRIEF**, the Applicant asserts that the claimed and prior art products are not identical, and that therefore there can be no presumption that claimed properties are functions are inherent. Thus Applicant reasserts that for the above reasons and those reasons presented in the **FIFTH SUPPLEMENTAL APPEAL BRIEF**, independent claim 14 is not anticipated by *Koshimizu '687* and demonstrated by *Mountsier* '933. Dependent claims 15, 16, and 19-21 ultimately depend from one of claim 14, and therefore include all of the limitations of the base claim. As such, *Koshimizu '687* as demonstrated by *Mountsier* '933 fails to anticipate claims 15, 16 and 19-21.

In regards to the Examiner's further argument that "[f]or an 'electrostatic force' to be used to hold a wafer and its support at an interface, a charge separation, or capacitance must be established per Coulomb's law and its related force equation." Claim 14 recites "the second electrode and the wafer providing a first capacitor of a high impedance, and the wafer and the ions in the enclosure providing a second capacitor of a low impedance, in a circuit *to produce a current of a low magnitude for etching the surface of the insulating layer in the wafer*" (Emphasis added). Applicants offer that an electrostatic chuck, which is vernacular for an electrode that uses electrostatic force to a wafer in position, does not act "in a circuit to produce a current of a low magnitude for etching the surface of the insulating layer in the wafer" as recited in claim 14, but rather provides for only immobility of the wafer.

B. Rejection of claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 under 35 U.S.C. 103(a) as being unpatentable over Koshimizu (5,980,687) in view of Mountsier et al. (5,810,933).

The Applicant reasserts that for the above reasons and those reasons presented in the **FIFTH SUPPLEMENTAL APPEAL BRIEF**, *Koshimizu '687* in view of *Mountsier '933* does not teach or suggest all of the limitations of independent claims 1, 7, 14 and 21, and therefore cannot render claims 1, 7, 14 and 21 unpatentable. Dependent

claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 ultimately depend from one of claim 1, 7, 14 and 21, and therefore include all of the limitations of the base claim. As such, *Koshimizu '687* in view of *Mountsier '933* does not teach or suggest all of the limitations of dependent claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51, and therefore cannot render dependent claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 unpatentable.

C. Rejection of claims 1-21, 43-51 under 35 U.S.C. 103(a) as being unpatentable over Applicant's own admitted prior art in view of Mountsier et al. (5,810,933).

The Applicant reasserts that for the above reasons and those reasons presented in the **FIFTH SUPPLEMENTAL APPEAL BRIEF**, Applicant's own admitted art (AAPA) in view of *Mountsier '933* does not teach or suggest all of the limitations of independent claims 1, 7, 14 and 21, and therefore cannot render claims 1, 7, 14 and 21 unpatentable. Dependent claims 2-6, 8-13, 15-20 and 43-51 ultimately depend from one of claim 1, 7, 14 and 21, and therefore include all of the limitations of the base claim. As such, AAPA in view of *Mountsier '933* does not teach or suggest all of the limitations of dependent claims 52-6, 8-13, 15-20 and 43-51, and therefore cannot render dependent claims 2-6, 8-13, 15-20 and 43-51 unpatentable.

VIII. CONCLUSION AND RELIEF

Based on the foregoing, Applicant requests that the Board overturn the Examiner's rejection of all pending claims and hold that the claims of the present application are allowable.

The Commissioner is hereby authorized to charge any deficiencies or credit overpayment to Deposit Account No. 26-1325.

Respectfully submitted,

Dated: 9/13/06

Michael L. Robbins
Attorney for the Applicant
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IX. CLAIMS APPENDIX.

Claims on Appeal:

1. (Previously Presented) In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition, a conduit for molecules of an inert gas,

a first electrode biased to a first voltage and spaced from the wafer,

a second electrode biased to a second voltage lower than the first voltage and spaced from the first electrode and the wafer and further spaced from the wafer than the first electrode,

magnetic members providing a magnetic field,

the first electrode and the magnetic members being disposed relative to each other and to the molecules of the inert gas for ionizing the molecules of the inert gas, and

the second electrode and the wafer being disposed relative to each other and to the ions of the inert gas, and the second electrode being constructed, to obtain a movement of the ions to the wafer at a low and controlled speed for an etching of the surface of the insulating layer by the ions at a low and controlled speed.

2. (Previously Presented) In a combination as set forth in claim 1,

a first member disposed adjacent the first electrode for providing a reference potential different from the bias on the first electrode to create a first electrical field, and

a second member disposed adjacent the second electrode for providing the reference potential to create a second electrical field,

the first electrical field and the magnetic field being disposed relative to each other and to the molecules of the inert gas from the supply for ionizing the molecules of the inert gas,

the second electrical field and the magnetic field being disposed relative to each other and to the ions of the inert gas to obtain the movement of the ions to the wafer at the low and controlled speed,

the second electrode being contiguous to, but spaced from, the wafer.

3. (Previously Presented) In a combination as set forth in claim 1,

a first source of alternating voltage for creating the bias on the first electrode, the bias on the first electrode being a negative direct voltage,

a second source of alternating voltage for creating the bias on the second electrode, the bias on the second electrode being a negative direct voltage,

the bias on the first electrode being less than the bias on the second electrode.

4. (Original) In a combination as set forth in claim 1,

the first electrode being disposed in a substantially parallel and contiguous relationship to the wafer,

there being a path for the flow of the argon molecules from the vicinity of the first and second electrodes and the magnetic members.

5. (Previously Presented) In a combination as set forth in claim 1,

the wafer being at a floating potential,

there being first and second electrically conductive members respectfully adjacent the first and second electrodes at a reference potential to provide for the creation of electrical fields respectively between the first electrode and the first electrically conductive member and between the second electrode and the second electrically conductive member.

6. (Previously Presented) In a combination as recited in claim 2,

a first source of alternating voltage for creating the bias on the first electrode, the bias on the first electrode being a negative direct voltage,

a second source of alternating voltage for creating the bias on the second electrode, the bias on the second electrode being a negative direct voltage,

the first electrode being disposed in a substantially parallel and contiguous relationship to the wafer,

there being a path for the flow of the molecules of the inert gas from the vicinity of the first and second electrodes and the magnetic members,

the wafer being at a floating potential,

there being first and second electrically conductive members respectfully adjacent, but spaced from, the first and second electrodes at a reference potential to provide for the creation of electrical fields respectively between the first electrode and the first electrically conductive member and between the second electrode and the second electrically conductive member.

7. (Previously Presented) In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition,

an enclosure defined by magnetic members forming a magnetic field and by first and second electrodes spaced from each other and from the wafers and providing electrical fields,

a supply of molecules of an inert gas for introducing the molecules into the enclosure,

a first source of an alternating voltage for producing a direct negative voltage of a high magnitude on the first electrode for the creation of a first electrical field of a high magnitude in the enclosure,

a second source of an alternating voltage for producing a direct negative voltage of a low magnitude on the second electrode for the creation of a second electrical field of a low magnitude in the enclosure,

the molecules of the inert gas in the enclosure being ionized by the combination of the electrical and magnetic fields, and

the wafer being disposed relative to the second electrode and relative to the ions of the inert gas in the enclosure to receive an etching of a low magnitude on the surface of the insulating layer by the ions of the inert gas in the enclosure.

8. (Previously Presented) In a combination as set forth in claim 7,

an opening in the enclosure for the flow of the molecules and ions of the inert gas from the enclosure,

the first source of the alternating voltage being operative to produce a direct voltage of the high magnitude and a negative polarity at the first electrode,

the second source of the alternating voltage being operative to produce a direct voltage of the low magnitude and a negative polarity at the second electrode,

the first electrode being disposed in contiguous, but spaced, relationship to the wafer.

9. (Previously Presented) In a combination as set forth in claim 7,

a first electrical conductor disposed in adjacent but spaced relationship to the first electrode at a particular reference potential to produce a first electrical field between the first electrode and the first electrical conductor, and

a second electrical conductor disposed in adjacent but spaced relationship to the second electrode at the particular reference potential to produce a second electrical field between the second electrode and the second electrical conductor.

10. (Original) In a combination as set forth in claim 7,

the wafer being disposed between the first and second electrodes in a substantially parallel relationship to the first and second electrodes and closer to the second electrode than the first electrode,

the wafer being at a floating potential relative to the negative potentials on the first and second electrodes and relative to the reference potential.

11. (Previously Presented) In a combination as set forth in claim 7,

the wafer being disposed in a spaced, but adjacent, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

12. (Original) In a combination as set forth in claim 10,

a vacuum pump for producing a vacuum in the enclosure, there being a space between the second electrode and the second conductive member for the flow of the molecules and ions of the inert gas from the enclosure.

13. (Previously Presented) In a combination as set forth in claim 10,

a first electrical conductor disposed in an adjacent, but spaced, relationship to the first electrode at a particular reference potential to produce a first electrical field between the first electrode and the first electrical conductor,

a second electrical conductor disposed in an adjacent, but spaced, relationship to the second electrode at the particular reference potential to produce a second electrical field between the second electrode and the second conductor,

the wafer being disposed in a spaced, but contiguous, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

14. (Previously Presented) In combination for etching an insulating layer in a wafer disposed in an enclosure to present a clean and fresh surface on the insulating layer for deposition,

magnetic members defining a magnetic field in the enclosure,

a first source of an alternating voltage for providing a first electrical field of a high magnitude in the enclosure,

a first electrode forming a part of the enclosure and connected to the first source of voltage for providing a negative DC voltage of a relatively high magnitude at a first position in the enclosure,

a second source of an alternating voltage for providing a second electrical field of a low magnitude in the enclosure,

a second electrode forming a part of the enclosure and connected to the second source of the alternating voltage for providing a negative DC voltage of a relatively low magnitude at a second position displaced from the first position and the wafer but near the wafer,

a conduit for introducing molecules of an inert gas into the enclosure for ionization by the combination of the electrical and magnetic fields to produce ions of high density,

the second electrode and the wafer providing a first capacitor of a high impedance, and the wafer and the ions in the enclosure providing a second capacitor of a low impedance, in a circuit to produce a current of a low magnitude for etching the surface of the insulating layer in the wafer.

15. (Previously Presented) In a combination as set forth in claim 14,

the first capacitor including a dielectric of the molecules and ions of the inert gas and the second capacitor including a dielectric constituting the insulating layer.

16. (Previously Presented) In a combination as set forth in claim 14,

a first electrically conductive member disposed in an adjacent but spaced relationship to the first electrode and having a reference potential to provide an electrical field between the first electrode and the first electrically conductive member, and

a second electrically conductive member disposed in an adjacent but spaced relationship to the second electrode and having the reference potential to provide an electrical field between the second electrode and the second electrically conductive member.

17. (Original) In a combination as set forth in claim 14,

the wafer having a floating potential and being disposed between the first and second electrodes in closer proximity to the second electrode than to the first electrode and being substantially parallel to the first and second electrodes.

18. (Previously Presented) In a combination as set forth in claim 17,

the conduit being disposed adjacent the first electrode to introduce the molecules of the inert gas into the enclosure and the molecules and ions of the inert gas being passed from the enclosure at a position adjacent to the second electrode.

19. (Previously Presented) In a combination as set forth in claim 14,

the magnetic members being disposed in a direction substantially perpendicular to the first and second electrodes to produce a helical movement of electrons in the enclosure and to provide for the production of the ions from the molecules of the inert gas by the electrons in the helical movement.

20. (Previously Presented) In a combination as set forth in claim 14,

a first electrically conductive member disposed in adjacent but spaced relationship to the first electrode and having a reference potential to provide an electrical field between the first electrode and the first electrically conductive member,

a second electrically conductive member disposed in adjacent but spaced relationship to the second electrode and having the reference potential to provide an electrical field between the second electrode and the second electrically conductive member,

the wafer having a floating potential and being disposed between the first and second electrodes in closer proximity to the second electrode than to the first electrode and being substantially parallel to the first and second electrodes,

the conduit being disposed adjacent, but spaced from, the first electrode to introduce the molecules of the inert gas into the enclosure and the molecules and ions of the inert gas being passed from the enclosure at a position adjacent to, but spaced from, the second electrode,

the magnetic members being disposed in a direction substantially perpendicular to the first and second electrodes to produce a helical movement of electrons in the enclosure and to provide for the production of the ions from the molecules of the inert gas by the electrons in the helical movement.

21. (Previously Presented) In combination for etching an insulating layer in a wafer to present clean and fresh surfaces on the insulating layer for deposition,

an enclosure

first and second electrodes disposed in the enclosure and displaced from each other and from the wafer for producing electrical fields in the enclosure, and

magnetic members disposed in the enclosure for producing a magnetic field in the enclosure in a direction transverse to the electrical field,

a first voltage source for producing a voltage of a high magnitude in the vicinity of the first electrode to obtain a production of a high electrical field in the enclosure,

a second voltage source for producing a voltage of a low magnitude in the vicinity of the second electrode to obtain a production of a low electrical field in the enclosure, and

a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and the magnetic members

in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and in obtaining a movement of the ions in the enclosure to the insulating layer in the wafer at a speed to obtain a smooth and uniform etching of the surface of the insulating layer at a low rate without any pits in the surface of the insulating layer.

22. (Withdrawn) A method of etching an insulating layer in a wafer to present a clean and fresh surface on the insulation layer for a deposition on the insulating layer, including the steps of:

providing a relatively strong electrical field at first positions in an enclosure,

providing a relatively weak electrical field at second positions displaced in the enclosure from the first positions, the relatively weak electrical fields defining a capacitor with a high impedance to limit the transfer of electrical charges to the insulating layer in the wafer,

passing molecules of an inert gas through the enclosure, and

providing a magnetic field in the enclosure in a direction relative to the strong electrical field to obtain a movement of electrons in the enclosure at the positions of the strong electrical field and an ionization of molecules of the inert gas by the electrons and a movement of the ions in a direction relative to the weak electrical field to obtain a movement of the ions, in accordance with the high impedance of the capacitor defined by the relatively weak field, to the second electrode at a speed for etching the surface of the insulating layer on the wafer substantially uniformly without pitting the insulating layer.

23. (Withdrawn) A method as set forth in claim 22 wherein

the relatively strong electrical field is provided in a first direction and the relatively weak electrical field is provided in a second direction opposite to the first direction and wherein

the magnetic field is provided in a direction transverse to the first and second directions to cooperate with the relatively strong electrical field in producing a movement of the electrons in the enclosure in a helical path for facilitating the ionization of molecules of the inert gas in the enclosure.

24. (Withdrawn): A method as set forth in claim 22

the wafer is disposed in the weak electrical field and wherein

the molecules of the inert gas are passed through the enclosure initially to positions in the relatively strong electrical field to obtain an ionization of molecules of the inert gas and subsequently through the enclosure to positions in the relatively weak electrical field to facilitate a substantially uniform etching of the surface of the insulating layer on the wafer by the ions.

25. (Withdrawn) A method as set forth in claim 22 wherein

the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak electrical field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the capacitor and a circuit including the capacitor for attracting the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

26. (Withdrawn) A method as set forth in claim 21 wherein

the capacitor constitutes a first capacitor and wherein

the relatively weak electrical field is defined by the first capacitor and a second capacitor in a series circuit and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and in which the plates of the first capacitor are separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the first capacitor and to provide the first capacitor with the high impedance and wherein

a second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates of the second capacitor are separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide the second capacitor with a relatively low impedance in comparison to the high impedance of the first capacitor.

27. (Withdrawn) A method as set forth in claim 26 wherein

the relatively strong electrical field is provided by a first electrode and a first alternating voltage providing a relatively high negative bias on the first electrode and wherein

the relatively weak electrical field is provided by a second electrode and by a second alternating voltage providing a relatively low bias on the second electrode.

28. (Withdrawn) A method as set forth in claim 26 wherein

the wafer is disposed in the relatively weak electrical field and wherein

the molecules of the inert gas are passed through the enclosure initially through positions in the relatively strong electrical field to obtain an ionization of molecules of the inert gas and subsequently through positions in the relatively weak electrical field to facilitate a substantially uniform etching of the surface of the insulating layer on the wafer by the ions and wherein

the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the first capacitor and a circuit including the second capacitor for attracting the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

29. (Withdrawn) A method as set forth in claim 26 wherein

the capacitor constitutes a first capacitor and wherein

the first capacitor and a second capacitor are in series and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and wherein

the plates of the first capacitor are separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the capacitor and to provide the high impedance and wherein

the second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates of the second capacitor are separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide a relatively low impedance in comparison to the high impedance of the first capacitor and wherein

the relatively strong electrical field is provided by a first electrode and a first alternating voltage providing a relatively high negative bias on the first electrode and wherein

the relatively weak electrical field is provided by a second electrode and by a second alternating voltage providing a relatively low negative bias on the second electrode.

30. (Withdrawn) A method of etching an insulating layer on a wafer to present a clean and fresh surface on the insulating layer for deposition, including the steps of

passing molecules of an inert gas through an enclosure,

disposing a first electrode in the enclosure to provide a strong electrical field in a first direction at first positions in the enclosure to ionize molecules of the inert gas in the enclosure,

disposing a second electrode in the enclosure to provide a weak electrical field at second positions in the enclosure in a second direction opposite to the first direction,

providing a magnetic field in the enclosure, in a direction transverse to the first and second directions, to cooperate with the strong electrical field in producing charged particles in the enclosure and to cooperate with the weak electrical field in producing a transfer of the charged particles to the surface of the insulating layer in the wafer to provide a weak and controlled etching of the surface of the insulating layer without producing pits in the surface of the insulating layer.

31. (Withdrawn) A method as set forth in claim 30 wherein

the molecules of the inert gas pass through the enclosure from the strong electrical field to the weak electrical field and wherein

the magnetic field is substantially perpendicular to the strong and weak electrical fields.

32. (Withdrawn) In a combination in claim 30 wherein

the strong electrical field is defined in part by the first electrode and by an alternating voltage applied at a first magnitude to the first electrode to bias the first electrode at a negative DC potential with a first magnitude and wherein

the weak electrical field is defined in part by the second electrode and by an alternating voltage applied to the second electrode at a second magnitude less than the first magnitude to bias the second electrode at a negative DC potential with a second magnitude less than the first magnitude for producing the transfer of the charged particles to the surface of the wafer to provide the weak and controlled etching of the surface of the insulating layer without producing pits in the surface of the insulating layer.

33. (Withdrawn) In a combination as set forth in claim 30 wherein

the magnetic field is provided by magnetic members and wherein

the magnetic members and the first and second electrodes define the enclosure.

34. (Withdrawn) In a combination as set forth in claim 30 wherein

the wafer is disposed in the weak electrical field and is separated from the second electrode in the weak electrical field.

35. (Withdrawn) In a combination as set forth in claim 30 wherein

the magnetic field is substantially perpendicular to the strong and weak electrical fields and wherein

the molecules of the inert gas pass into the enclosure through the strong magnetic field and the molecules and the ions of the inert gas pass from the enclosure through the weak electrical field.

36. (Withdrawn) A method as set forth in claim 30 wherein

the second electrode and the wafer constitute plates of a first capacitor and ions and molecules of the inert gas constitute the dielectric of the first capacitor and wherein

the wafer and the ions of the inert gas constitute plates of a second capacitor and wherein the insulating layer of the wafer constitutes the dielectric of the second capacitor and wherein

the first capacitor has a higher impedance than the second capacitor.

37. (Withdrawn) A method of etching an insulating layer on a wafer having at least one socket, defined by walls in the insulating layer, to present a clean and fresh surface on the insulating layer, including the walls of the socket, for deposition, including the steps of:

passing molecules of an inert gas through an enclosure,

providing a strong electrical field at first positions in the enclosure to ionize molecules of the inert gas in the enclosure

providing a weak electrical field at second positions, including the positions of the wafer, in the enclosure, and

providing a magnetic field in the enclosure in a direction transverse to the directions of the first and second electrical fields in the enclosure to cooperate with the strong electrical field in producing charged particles and to cooperate with the weak electrical field in producing a transfer of the charged particles, to the surface of the insulating layer in the wafer and to the walls of the socket in the insulating layer, at a low speed to provide a weak and controlled etching of a uniform thickness from the surface of the insulating layer and the walls of the socket without pitting the surface of the insulating layer or the walls of the socket.

38. (Withdrawn) A method as set forth in claim 37, including the steps of:

providing a first electrode in the enclosure for the strong electrical field and introducing an alternating voltage of a first particular amplitude to the first electrode to produce a strong negative DC bias on the first electrode for the creation of the strong electrical field,

providing a second electrode in the enclosure for the weak electrical field and introducing an alternating voltage of a second particular amplitude less than the first particular amplitude to the second electrode to produce a weak negative DC bias on the second electrode for the creation of the weak electrical field.

39. (Withdrawn) A method as set forth in claim 37, including the steps of:

disposing the wafer in the enclosure in an adjacent but spaced relationship to the second electrode to provide a high impedance between the second electrode and the wafer for limiting the transfer of charged particles to the surface of the insulating layer and the walls of the socket and for providing for a removal of a substantially uniform thickness from the surface of the insulating layer and from the surfaces of the walls of the socket.

40. (Withdrawn) A method as set forth in claim 37 including the steps of:

providing a first electrode to create the strong electrical field,

providing a second electrode to create the weak electrical field,

providing magnets to create the magnetic field,

the first and second electrodes and the magnets substantially defining the enclosure, and

disposing the wafer in the enclosure in a closely spaced relationship to the second electrode.

41. (Withdrawn) A method as set forth in claim 37 wherein

the wafer is at a floating potential and wherein

the magnets are substantially at a ground potential and wherein

first and second members substantially at ground potential are provided respectively in proximity to the first and second electrodes to cooperate respectively with the first and second electrodes in creating the strong and weak electrical fields.

42. (Withdrawn) A method as set forth in claim 37 including the steps of:

introducing an alternating voltage of a first particular magnitude to the first electrode to produce a strong negative DC bias on the first electrode for the creation of the strong electrical field,

introducing an alternating voltage of a second particular magnitude less than the first particular magnitude to the second electrode to produce a weak negative bias on the second electrode for the creation of the weak electrical field, and

providing a high impedance between the second electrode and the wafer and a low impedance between the wafer and the charged particles near the wafer to produce a transfer of charged particles with limited energy to the surface of the insulating layer and the walls of the socket in the insulating layer and to provide the weak and controlled etching of the surface of the insulating layer and the walls of the socket with a substantially uniform thickness of material from the insulating layer and the wall of the socket without pitting the surface of the insulating layer or the walls of the socket.

43. (Previously Presented) In a combination as set forth in claim 21 wherein,

the first electrode provides the high electrical field in cooperation with the magnetic field for producing an ionization of molecules of an inert gas in the enclosure and wherein

the second electrode provides the low electrical field in cooperation with the magnetic field for etching the surface of the insulating layer on the wafer to obtain the smooth and uniform etching on the surface of the insulating layer at the low rate without any pits in the surface of the insulating layer.

44. (Previously Presented) In a combination as set forth in claim 21 wherein

the first voltage source applies an alternating voltage from the voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and wherein

the second voltage source applies an alternating voltage from the second voltage source to the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode.

45. (Previously Presented) In a combination as set forth in claim 21 wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in a cooperative relationship with the second electrode to provide for the production of the low electrical field.

46. (Previously Presented) In a combination as set forth in claim 45 wherein

the first and second electrodes are substantially parallel to the wafer and wherein

the first and second electrical conducting members are substantially parallel to the first and second electrodes.

47. (Original) In a combination as set forth in claim 46 wherein

the first and second electrical conducting members are respectively disposed in a substantially parallel, but spaced, relationship to the first and second electrodes.

48. (Previously Presented) In a combination as set forth in claim 43 wherein

the wafer and the first electrode define a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and wherein the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer.

49. (Previously Presented) In a combination as set forth in claim 47 wherein,

the wafer and the first electrode define a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and wherein the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer.

50. (Previously Presented) In a combination a set forth in claim 44 wherein

a first electrical conducting member is disposed in cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in cooperative relationship with the second electrode to provide for the production of the low electrical field.

51. (Previously Presented) In a combination as set forth in claim 49 wherein

the first voltage source applies an alternating voltage from the first voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and wherein

the second voltage source applies an alternating voltage from the source to the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode wherein

a first electrical conducting member is disposed in cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in cooperative relationship with the second electrode to provide for the production of the low electrical field.

X. EVIDENCE APPENDIX.

None

XI. RELATED PROCEEDING APPENDIX.

None